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Understanding Latch-Up in Advanced CMOS Logic

Latch-up has long been a bane to CMOS IC applications; its occurrence and theory have been the subjects of numerous studies and articles. The applications engineer and systems designer, however, are not so much concerned with the theory and modeling of latch-up as they are with the consequences of latch-up and what has been done by the device designer and process engineer to render ICs resistant to latch-up.

Of equal interest are those precautions, if any, which must be observed to limit the liability of designs to latch-up.

WHAT IS LATCH-UP?

Latch-up is a failure mechanism of CMOS integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction. It may be a temporary condition that terminates upon removal of the exciting stimulus, a catastrophic condition that requires the shutdown of the system to clear or a fatal condition that requires replacement of damaged parts. Regardless of the severity of the condition, latch-up is an undesirable but controllable phenomenon. In many cases, latch-up is avoidable.

The cause of the latch-up exists in all junction-isolated or bulk CMOS processes: parasitic PNPN paths. Figure 1, a basic N-subtrate CMOS cross section, shows the parasitic NPN and PNP bipolar transistors which most frequently participate in latch-up. The P+ sources and drains of the P-channel MOS devices act as the emitters (and sometimes collectors) of lateral PNP devices; the N-substrate is the base of this device and collector of a vertical NPN device. The P-well acts as the collector of the PNP and the base of the NPN. Finally, the N+ sources and drains of the N-channel MOS devices serve as the emitter of the NPN. The substrate is normally connected to V_{CC}, the most positive circuit voltage, via an N+ diffusion tap while the P-well is terminated at GND, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and P-well.

Similarly, Figure 2, a basic P-substrate CMOS cross section, shows the parasitic PNP and NPN bipolar transistors which most frequently participate in latch-up. The N+ sources and drains of the N-channel MOS devices act as the emitters (and sometimes collectors) of lateral NPN devices; the P-substrate is the base of this device and collector of a vertical PNP device. The N-well acts as the collector of the NPN and the base of the PNP. Finally, the N+ sources and drains of the P-channel MOS devices serve as the emitter of the PNP. The N-well is normally connected to V_{CC}, the most positive circuit voltage, via an N+ diffusion tap while the substrate is terminated at GND, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and N-well.

Although the rest of this application note will refer to the N-substrate model, the same discussion is true for the P-substrate model, as illustrated by Figure 1, Figure 2.

Normally, only a small leakage current flows between the substrate and P-well causing only a minute bias to be built up across the bulk due to the resistivity of the material. In this case the depletion layer formed around the reverse-biased PN junction between P-well and the substrate supports the majority of the V_{CC}-GND voltage drop. As long as the MOS source and drain junctions remain reverse-biased, CMOS is well behaved. In the presence of intense ionizing radiation, thermal or over-voltage stress, however, current can be injected into the PNP emitter-base junction, forward-biasing it and causing current to flow through the substrate and into the P-well. At this point, the NPN device turns on, increasing the base drive to the PNP. The circuit next enters a regenerative phase and begins to draw significant current from the external network thus causing most of the undesirable consequences of latch-up. Once established, a latch-up site, through the fields generated by the currents being conducted, may trigger similar action in both elements of the IC.
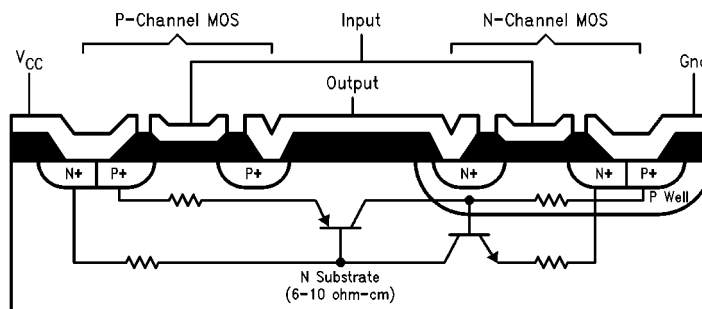

FIGURE 1. Basic CMOS Inverter Cross Section with Latch-Up Circuit Model
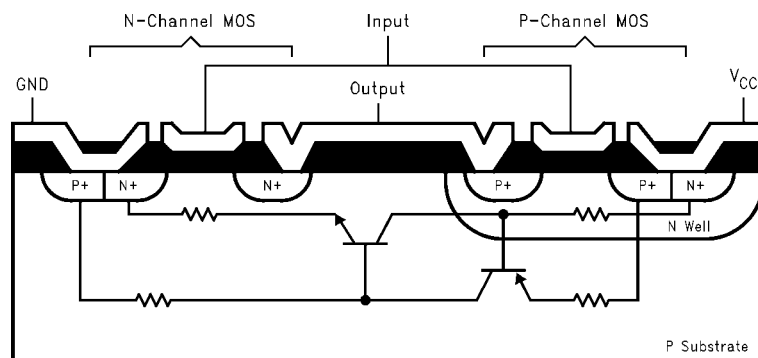
FIGURE 2. Basic P-Substrate CMOS Inverter Cross Section with Latch-Up Circuit Model

WHAT TO DO

As might be expected, latch-up is highly dependent on the characteristics of the bipolar devices involved in the latch-up loop. Device current gains, emitter efficiencies, minority carrier life times and the degree of NPN-PNP circuit coupling are all important factors relating to both the sensitivity of the particular latch-up device and to the severity of the failure once it has been excited. Layout geometry and process both contribute significantly to these parameters; CMOS, like other technologies, has been shrunk to provide more function per unit area, increasing susceptibility to latch-up. All major CMOS vendors have upgraded their processes and/or design rules to compensate for this increased susceptibility, some with more success than others. The lateral PNP is typically the weak link in the latch-up loop. As such, various devices can be exploited toward reducing the effectiveness of the PNP to participate in latch-up. Guard banding, device placement, the installation of pseudo-collectors between the P-channel devices and the P-well, and the use of a low resistivity substrate under an epitaxial layer are a few of the IC design tactics now being practiced to reduce the current gain or to control the action of the lateral PNP structures in state-of-the-art CMOS devices.

Vendors of CMOS ICs have always been aware of the latch-up phenomenon and have considerably improved their designs and processes to reduce the danger of latch-up occurring under normal usage. Abnormal applications and misuse of CMOS ICs may still pose problems that the CMOS vendor has little control over. Hence, CMOS users must be aware of what they are doing and those measures which must be taken to reduce the susceptibility to latch-up. The use of CMOS at or beyond its rated maximum voltage range and the presence of inductive transients are applications-related situations which can trigger latch-up. Environment, including thermal stress, poorly regulated or noisy supplies and radiation incidence can also contribute to or cause latch-up. The system engineer must consider these situations when using CMOS in designs.

While latch-up is generally recognized as resulting from regenerative switching along a PNPN path, many designers incorrectly assume that this regenerative action places the device in a state that can only be recovered from if the system is powered down. The fact is that there is probably an equal, if not greater, chance that the regenerative switching, when encountered, will be non-sustaining (the condition, more accurately referred to as current amplification, will disappear when the triggering stimulus is removed); over-voltage applied to properly designed input protection networks is one example of controlled current amplification. For sustained latch-up to occur, the regeneration loop must have sufficient gain and the power source must be able to supply a minimum current. From this we can see that current-limited power supplies might be used to recover from or reduce the effects of latch-up. Another method uses current-limiting series resistors in the power connections of offending ICs in conjunction with storage capacitors shunting the devices. Normal switching current will be drawn from the capacitors while DC current will be limited by the resistors.

In the loop of positive current feedback formed by the parasitic PNP and NPN transistors of the latch-up structures, regenerative switching may result if sufficient loop gain is available. One must remember, though, that three conditions are necessary for latch-up to occur.

1. both parasitic bipolars must be biased into the active state;
2. the product of the parasitic bipolar transistor current gains ($B_{npn} \cdot B_{pnp}$) must be sufficient to allow regeneration, i.e., greater than or equal to one;
3. the terminal network must be capable of supplying a current greater than the holding current required by the PNPN path. In processes utilizing an epitaxial silicon, this current is usually in excess of 1A.

If any of these conditions is not met both during the initiation and in the steady state, then the latch-up condition is either non-sustaining or cannot be initiated. If the current to the latched structure is not limited, permanent damage may result. Again, any means to prevent any of these conditions from being satisfied will protect the circuit from exhibiting sustained latch-up.

The prevention of biasing the bipolars into the active region and the limiting of the current which may be supplied by the network are the two factors which system designers have under their control. Many of the protective measures long exercised in discrete and TTL designs may also be applied to CMOS designs to reduce susceptibility and prevent damage to these systems. Diode clamping of inductive loads, signal and supply level regulation, and sharing of large DC loads by several devices with suitable series limiting resistors to distribute thermal stress over a larger area or multiple ICs are all positive-preventive measures to exploit.

While we have been considering the CMOS device in a generic manner, there are two primary structures used in all CMOS ICs which have latch-up paths associated with them; these are the inverter or gate and the transmission

switch. Both structures may be susceptible under the right conditions. While the CMOS inverter can exhibit latch-up independent of circuit configuration, the transmission switch usually has lower holding current, and thus, a lower threshold for latch-up, but is dependent on its external connections for latch-up to occur. Figure 3 shows the lumped equivalent circuit of the N-substrate inverter. Figure 4 shows the same lumped equivalent circuit of the P-substrate inverter. Notice the shunting resistors across the base-emitter junctions of the bipolar transistors: these resistors divert base drive from the bipolars and as a result increase both the trigger current and holding current levels required for the structures to participate in latch-up. A further increase in these current levels can be achieved by further decreasing the shunt resistance. Diffusing all active components into an epitaxial silicon, under which would lie a substrate of substantially less resistivity, will have a dramatic effect on decreasing the shunt resistance, therefore increasing the trigger current and holding current levels required for latch-up.
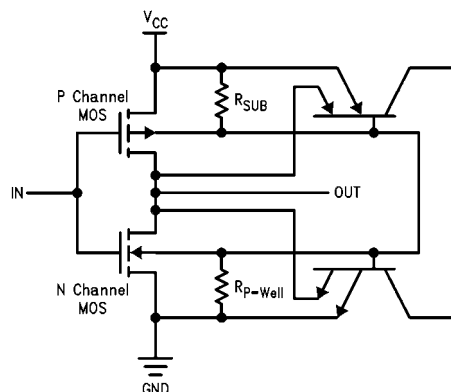

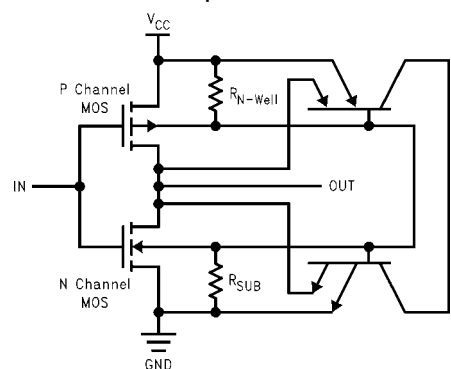FIGURE 3. N-Substrate CMOS Inverter with Parasitic Bipolars

FIGURE 4. P-Substrate CMOS Inverter with Parasitic Bipolars

THE CIRCUIT CONNECTION

As we have seen above, the external circuit connections are regular participants in the latch-up process. The current for latch-up comes from these connections and often the triggering mechanism is external to the latching device. All three classes of external connections (power, input and output) are important in latch-up. We will now look at how these connections relate to this process.

Current injection through the power terminals when the power supply voltage is beyond the maximum rated for the CMOS device can directly cause latch-up through base collector leakage or breakdown mechanisms. One aspect of high power supply voltages that is not often recognized is the effect of field-aiding lateral currents under the emitters of the PNP devices. This can effect a significant increase in the beta of these devices, making internally trigger latch-up much more prevalent. Again, the warning to the system designer is to avoid using CMOS at maximum rated supply voltages unless precautions are taken to insure latch-up is unlikely or is at least acceptable and recoverable. Switching transients coupled onto power lines has become a problem now that CMOS has become a high-speed logic technology. Attention to power supply decoupling is now a necessity when designing with high-speed CMOS. Of course, CMOS processes incorporating an epitaxial silicon over a substrate of very low resistivity is less prone to latch-up under these conditions. These recommended precautions should be taken just the same.

Latch-up involving input terminals, next to gate oxide rupture, used to be one of the most common failure mechanisms of CMOS. Transients exceeding the power supply routinely caused either or both of these effects to occur. Fortunately, CMOS vendors have learned to make better input protection networks and have learned that proper placement of these components with respect to the rest of the chip circuitry is necessary to reduce susceptibility to latch-up. The system designer should review foreign input signals to CMOS systems and take precautions necessary to limit the severity of over/undershoot from these sources. Measures which could be used to reduce the possibility of latch-up induced by input signals are: proper termination of transmission lines driving CMOS, series current limiting resistors, AC coupling with DC restoration to the CMOS supplies, and the addition of Schottky diode clamps to the CMOS power rails. As an additional measure there are several CMOS circuits which have input protection networks that can handle over voltage in one direction or the other and which are specifically designed to act as interface circuits between other logic families and CMOS. Judicious application of these will also aid in suppressing any tendencies of CMOS systems to latch-up.

Finally, attention to CMOS outputs, their loading and the stresses applied to them will also enable the designer to generate latch-up free systems. Historically, output terminals of CMOS have been least likely to cause latch-up though they can participate in latch-up once it is initiated. The normal mode of failure in this respect is, again, the application of voltages beyond the CMOS supplies or the maximum limit for the devices though excessive current has also been linked to latch-up failure at elevated temperatures. Inductive surges and transmission line reflections are the most likely sources of output latch-up in CMOS and should be attended to in the most applicable method, i.e., by clamping, termination or through dissipative measures.

WHAT WE HAVE DONE

Fairchild Semiconductor, as an important supplier of advanced CMOS to all segments of the industry, has made a commitment to provide IC designs which make use of state-of-the-art latch-up suppression techniques in an effort to support its customers before they need support. The three most important actions which we have taken to guard our customers from latch-up are in the areas of layout, power distribution and process design. These techniques,

along with recognized good design practice, yield a product line that lives up to the intent of an advanced CMOS family. In brief review, Fairchild Semiconductor's attack on latch-up is summarized in the following.

Latch-Up Protection Geometries

Every FACT™, VHC, and LCX IC employs special geometries to isolate every input protection device and every output from active areas on the chip. In this way, structures which would normally participate in latch-up loops are decoupled and are thus less troublesome. All devices are scrutinized for potential latch-up sites and are protected by similar geometries where any risk is significant.

Power Distribution

Careful attention to on-chip power distribution and enhanced termination of P-wells or N-wells and substrate is used by Fairchild Semiconductor to improve latch-up resistance. Our metal process affords the advantage in maintaining low impedance distribution of power and ground potentials over the entire chip; the potential gradient-caused fields which often induce or enhance latch-up are thus minimized while functional performance is enhanced by cleaner on-chip power supplies.

Process Design

By design, the FACT, VHC, and LCX processes are better both in low latch-up susceptibility and in enhanced device performance. The most significant advancement of these processes has been the incorporation of an epitaxial silicon layer. Figure 5 illustrates a modified version of Figure 1, uti-

lizing an epitaxial layer of silicon to contain all of the active components of the CMOS circuit. This epitaxial layer allows the use of a separate layer of substrate silicon, of a resistivity some three orders of magnitude lower than the epitaxial layer. The effect is also modeled in Figure 5.

As illustrated, the resistivity of the epitaxial silicon, R_1, is on the order of 6 ohm-cm to 10 ohm-cm. The underlying substrate resistivity, R_2, is as low as 0.008 ohm-cm to 0.025 ohm-cm. The result is a parallel combination of resistivities, R_1 and R_2, that is equivalent to R_2. What has now happened is that the gain of the parasitic PNP-NPN circuit has been dramatically slashed. Under the same latch-up conditions described earlier, the introduction of the low resistivity substrate now means that at least 10 times more current is needed to trigger the parasitic PNP-NPN combination.

The active components within the epitaxial layer maintain the same performance characteristics as those of the active area illustrated in the non-epitaxial CMOS circuit of Figure 1. Therefore the introduction of the epitaxial layer to the FACT,VHC, and LCX processes does not reduce any AC, DC, functional or ESD performance. However, what we have are advanced CMOS logic families that are now virtually latch-up immune.

Thus, through innovative and careful layout, attention to eliminating circuit situations which could be latch-up prone and by careful selection and maintenance of our advanced CMOS process, FACT, VHC, and LCX set the standard for latch-up resistance.
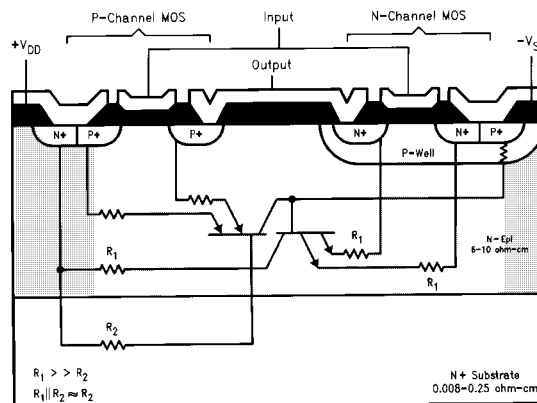

FIGURE 5.

LIFE SUPPORT POLICY

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